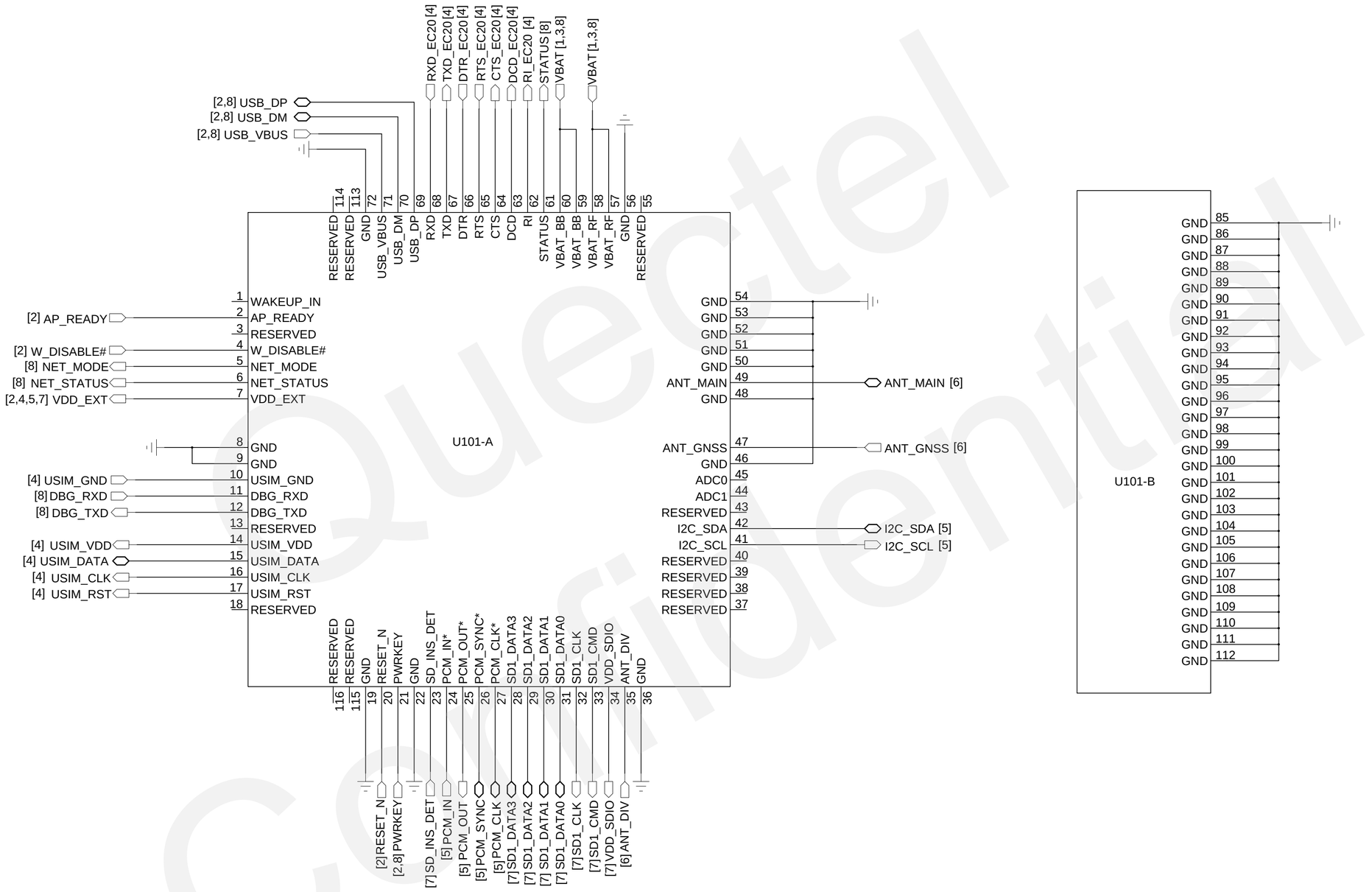
Module Interface

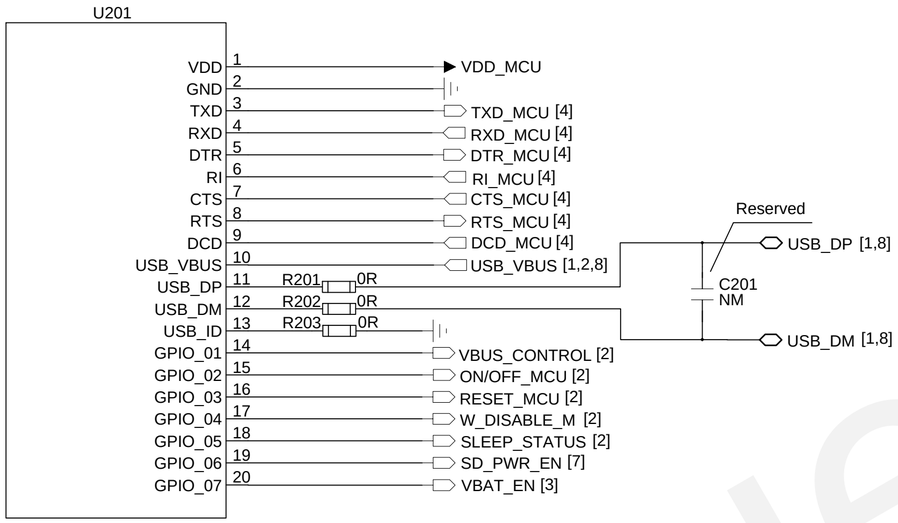


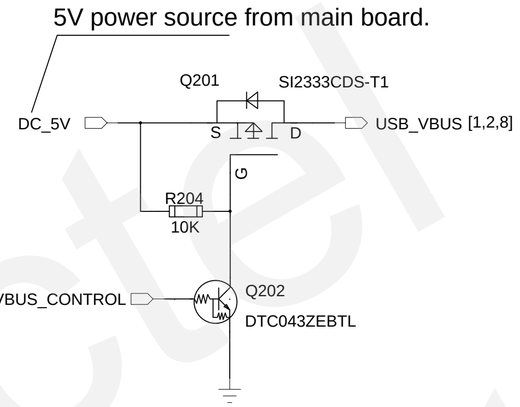
Notes:

1. Keep all RESERVED and unused pins unconnected.
2. Pin 73~84 and 117~140 are unused in the design. You can ignore them in schematic and PCB decal.
3. The DBG_RXD/DBG_TXD, CTS/RTS/DCD and SD functions are not supported on EC20-E currently.

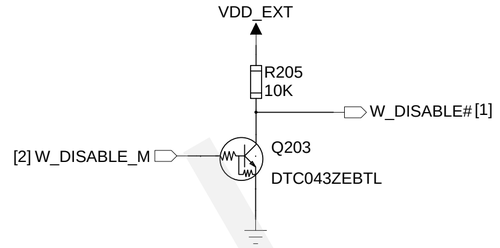
Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE Module Interface
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 1 OF 8	DATE 2015/3/30

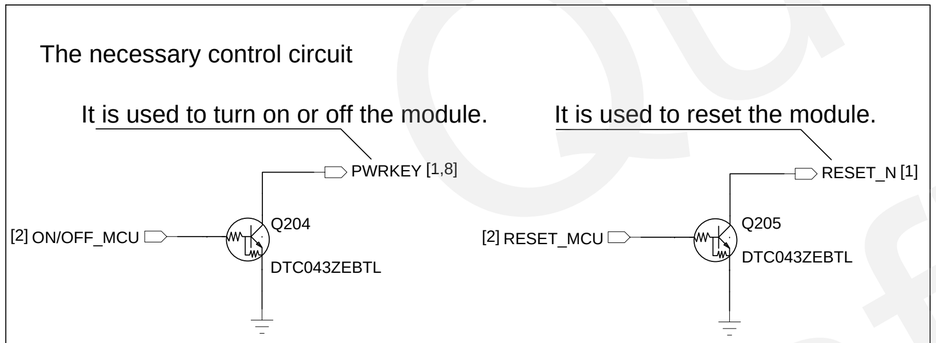
MCU Interface

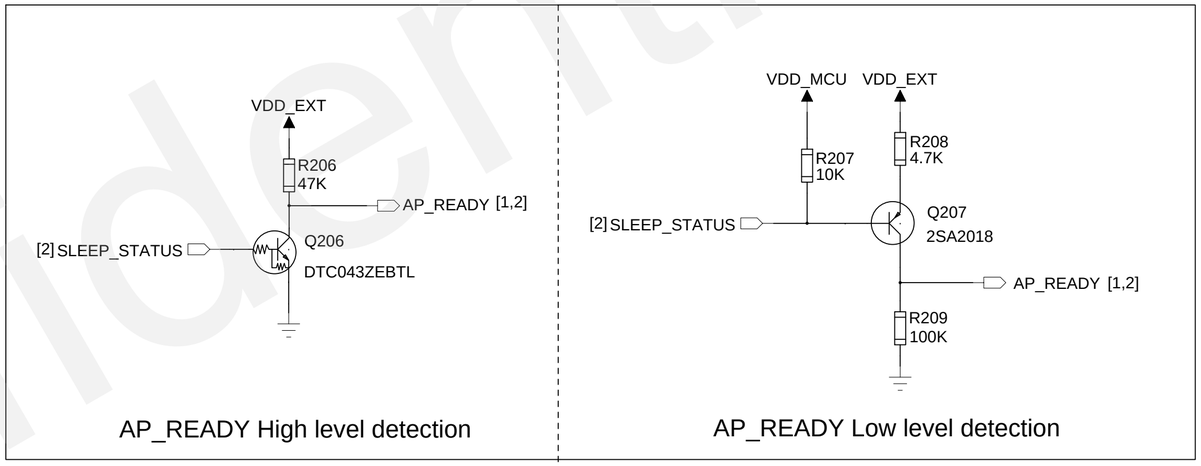




VBUS_CONTROL = High level, Q201 conducts.







Notes:

1. U201 represents customer's MCU.
2. EC20 can only work as a USB device and support FS/HS mode. To communicate with USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and EC20 need to be provided by 5V power for USB detection, and VBUS_CONTROL turns on and off VBUS power supply.
3. AP_READY can be configured to high level detection and low level detection. For more details about AP_READY, please refer to the document <Quectel_EC20_Hardware_Design> and <Quectel_EC20_AT_Commands_Manual>.
4. Transistor circuits (Q203~Q207) are used for level translation.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE MCU Interface
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 2 OF 8	DATE 2015/3/30

Power Supply Design

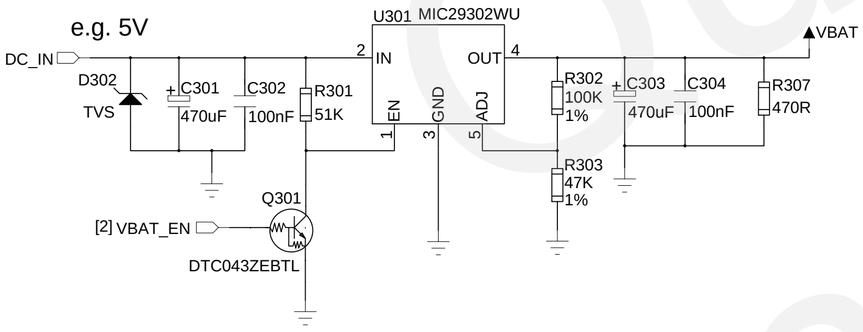
DC-DC Application

It is used when the input voltage is above 7V. Use DC-DC to convert high input voltage to 5V, and LDO will generate 3.8V typical voltage for the module.

e.g. DC12V IN → DC-DC → DC 5V out → LDO → DC 3.8V out for module

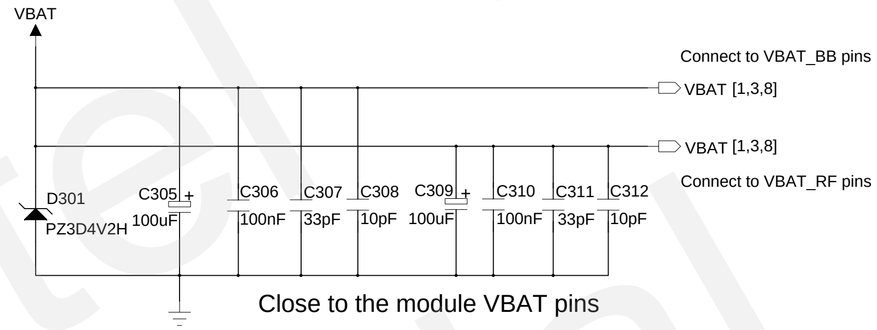
LDO Application

It is used when the input voltage is below 7V.



VBAT = (R302/R303+1)*1.24 = 3.88V

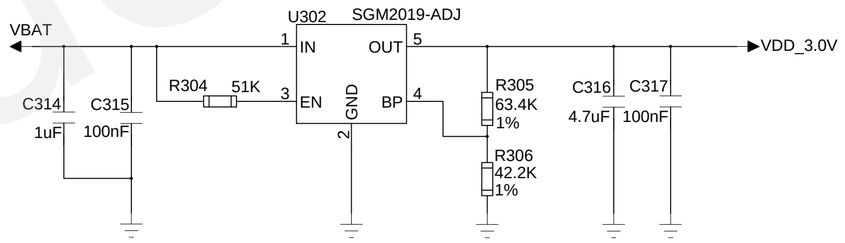
VBAT Design



Note:

VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.

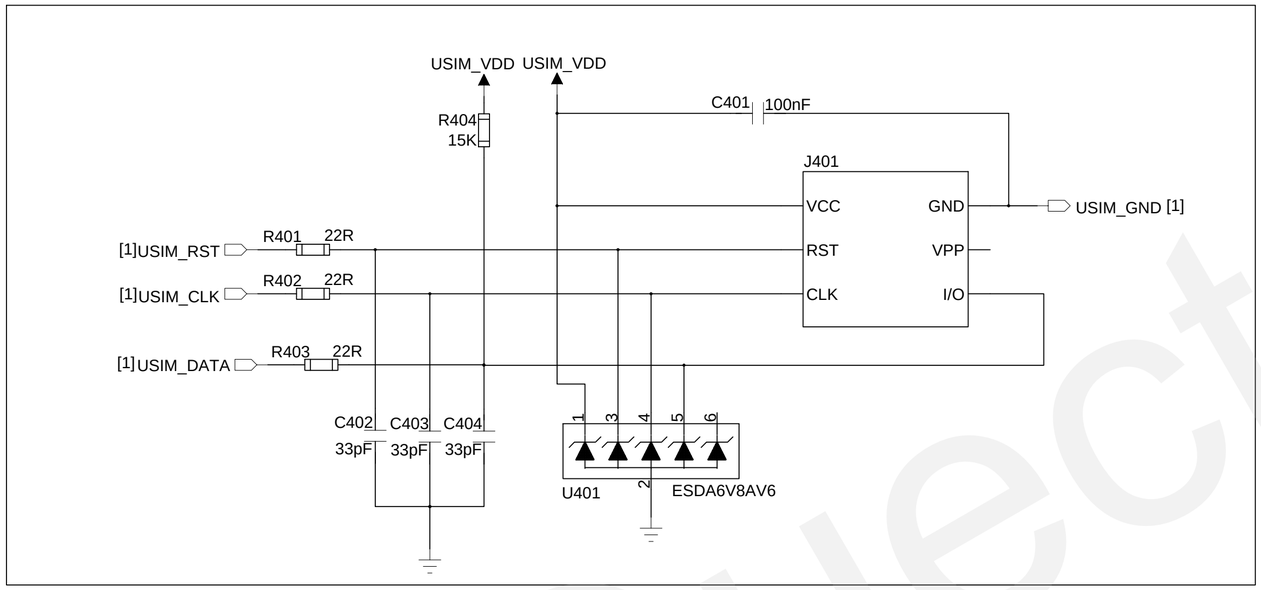
Supply Power for PCM Codec and SD Card



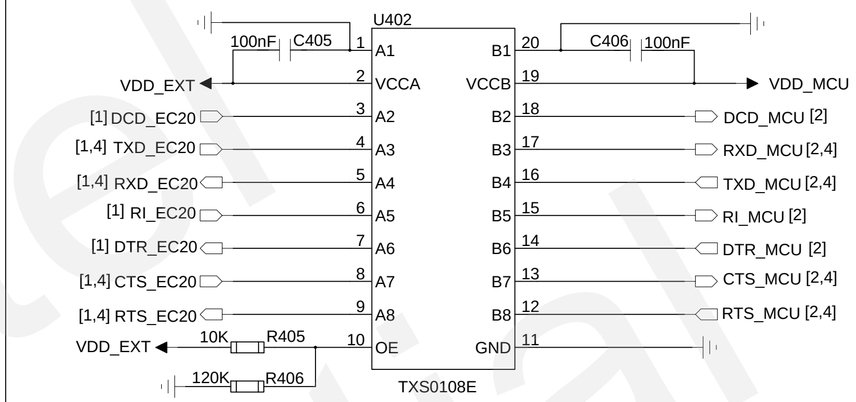
VDD_3.0V = (R305/R306+1)*1.207 = 3.0V

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE Power Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 3 OF 8	DATE 2015/3/30

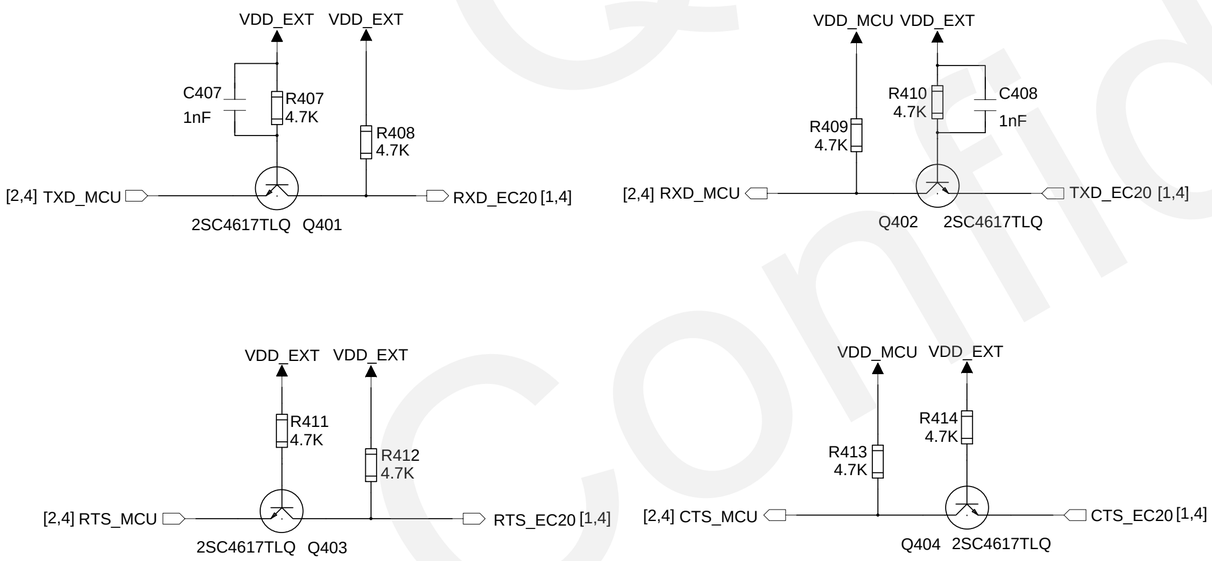
USIM and UART Design



UART Translation IC Solution



UART Transistor Solution (Recommend)

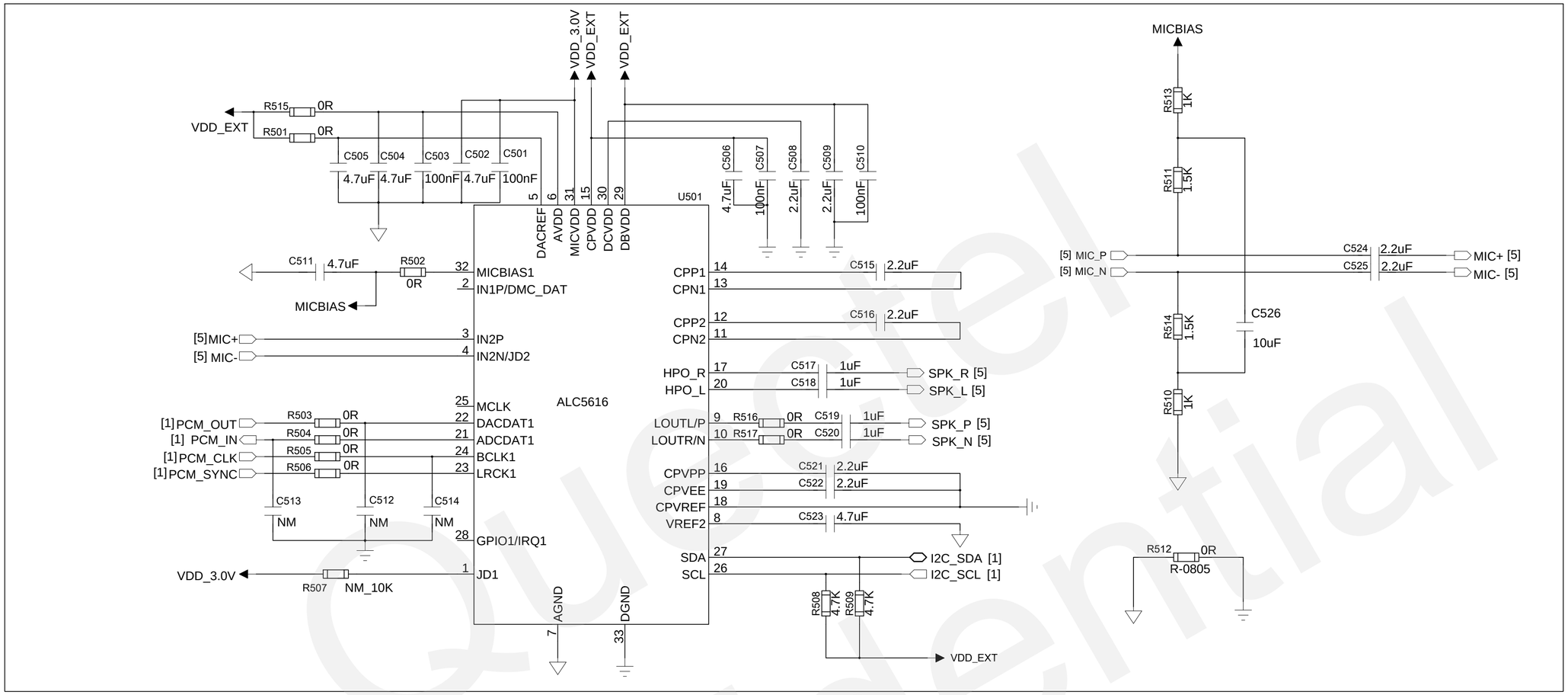


Notes:

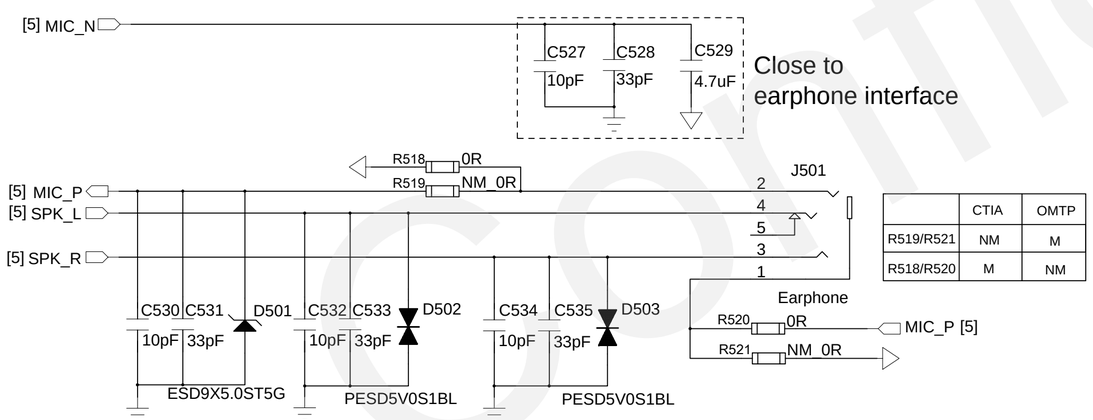
1. R401~R403 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
2. R404 can improve anti-jamming capability of the USIM circuit, and it should be placed close to the USIM connector.
3. VCCA should not exceed VCCB. For more information about TXS0108E, please refer to the datasheet from TI.
4. If you need to enable high baud rate, it is highly recommended to install a 1nF capacitor (C407/C408) on transistor circiut.
5. The DTR transistor circuit is similar with RTS interface, and the RI and DCD transistor circuit is similar with CTS interface.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE USIM and UART Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 4 OF 8	DATE 2015/3/30

Audio Design

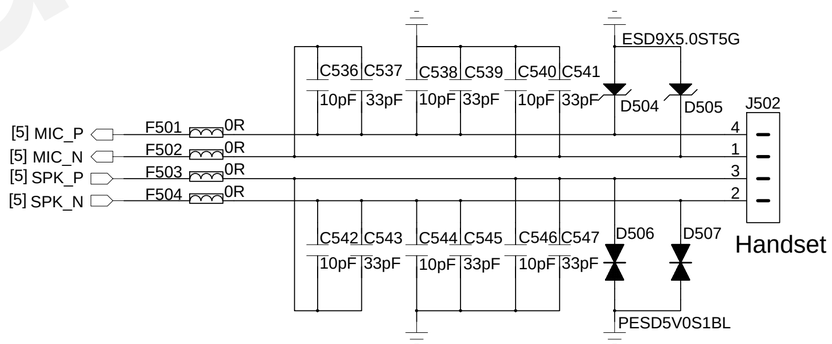


Audio - Earphone Application



	CTIA	OMTP
R519/R521	NM	M
R518/R520	M	NM

Audio - Handset Application

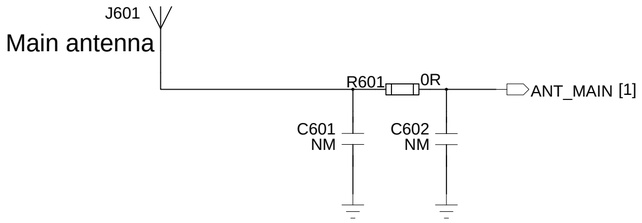


Note: It is needed to add audio amplifer when the speaker impedance is less than 32ohm.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE Audio Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 5 OF 8	DATE 2015/3/30

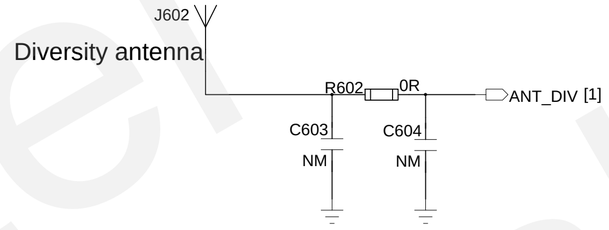
RF and GNSS Design

Main Antenna Interface



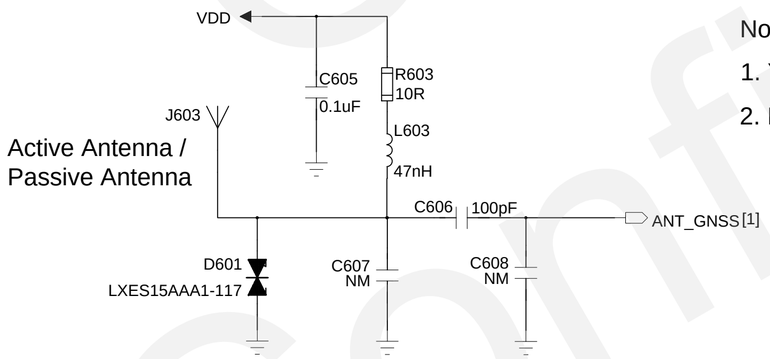
C601 and C602 are reserved for impedance matching.

Diversity Antenna Interface



C603 and C604 are reserved for impedance matching.

GNSS Antenna Circuit

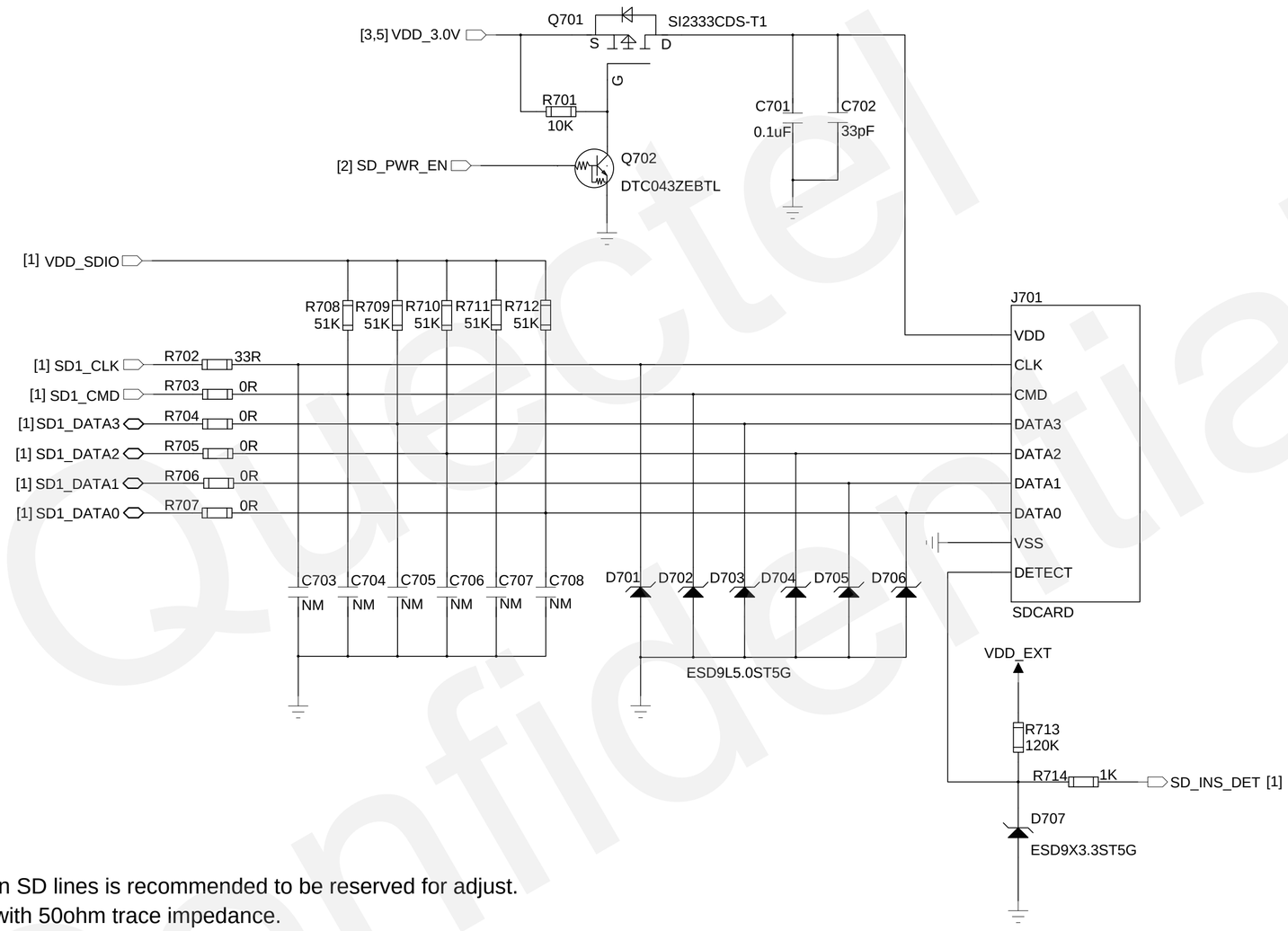


Notes:

1. You can choose an external LDO according to the active antenna to supply power (VDD left).
2. If you design the antenna circuit with passive antenna, the R603 and L603 are not needed.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE RF and GNSS Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 6 OF 8	DATE 2015/3/30

SD Design



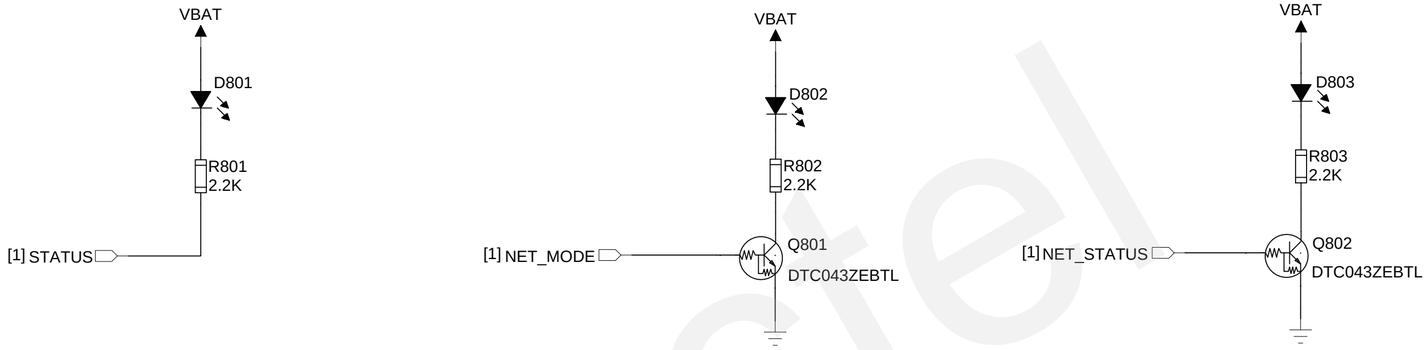
Notes:

1. The RC circuit on SD lines is recommended to be reserved for adjust.
2. Route SD lines with 50ohm trace impedance.
3. Total routing length < 100mm is recommended.
4. Spacing to all other signals with more than 2x line width.
5. The parasitic capacitance of ESD components should be smaller than 15pF.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	**PROJECT** EC20 Reference Design	**TITLE** SD Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 7 OF 8	DATE 2015/3/30

Indicator and Test Point

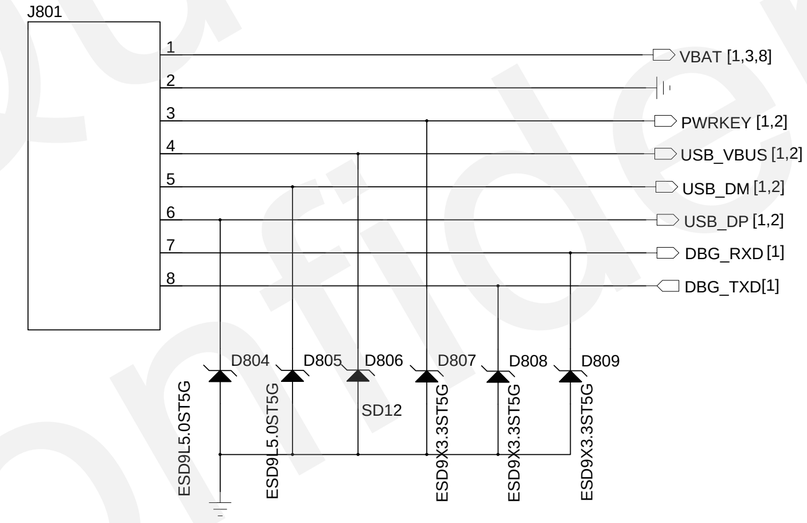
Indicators



Notes:

1. Module STATUS is open drain output.
2. Refer to the document <Quectel_EC20_Hardware_Design> for more details about NET_MODE and NET_STATUS.

Reserved Test Points



Notes:

1. Both USB and debug UART interface are reserved for software debug.
2. USB interface can be used to upgrade firmware either.
3. Keep USB test points as close as possible to USB pins.

Quectel Wireless Solutions		
DRAWN BY Mountain.ZHOU	PROJECT EC20 Reference Design	TITLE Other Design
CHECKED BY Radom.XIANG	SIZE A2	VER 1.0
	SHEET 8 OF 8	DATE 2015/3/30