dLAN® Green PHY eval board II

Data sheet

DESCRIPTION
This Evaluation Board is designed for the dLAN® Green PHY Module.
It provides PLC to a mains-line or to twisted pair connectors and gives the access to many of the available interfaces like Ethernet, USB, RS232 and more functionality on several PinHeaders.
The Evaluation Board provides two mikroBUS® slots for use with all the IO-modules available as CLICK® boards designed by MikroElektronika (http://www.mikroe.com/click).

SCOPE OF FUNCTIONALITY
The default functionality of the board is bridging from PLC to Ethernet. For all other kinds of applications and driving other interfaces or expansion slots specific firmware has to be adapted by means of the dLAN® Green PHY SDK.

FEATURES
- Evaluation board for dLAN® Green PHY Module
- PLC over mains-line or twisted pair connection
- Board is powered by micro-USB-Connector
- Standard JTAG and serial debug ports
- PLC <-> Ethernet bridging
- Two expansion slots for mikroBUS IO-Modules
- One General Purpose Port with digital or analog I/O

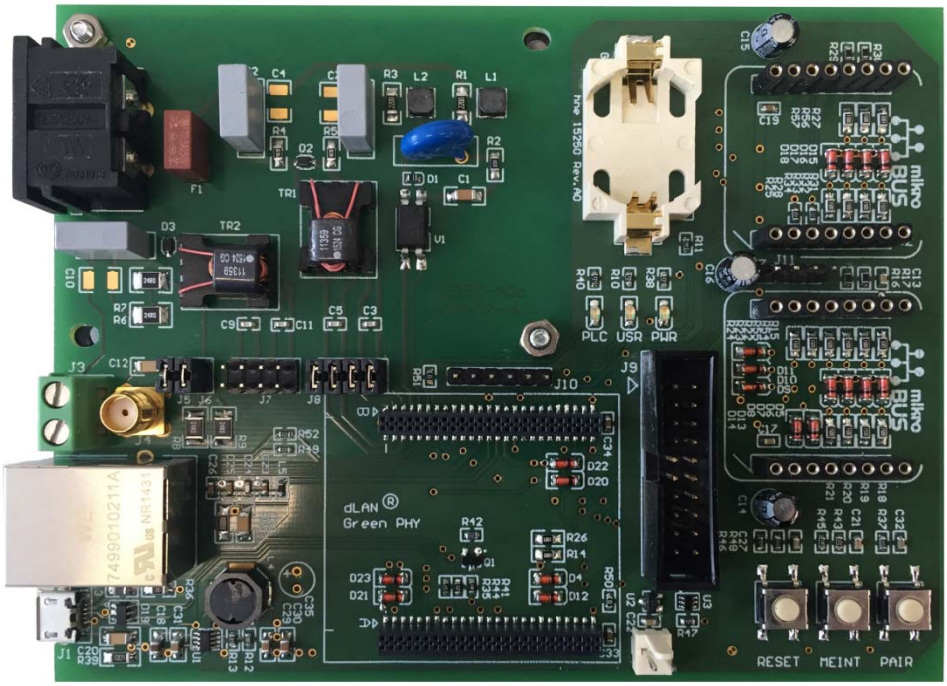

Fig 1: Picture of the devolo dLAN® Green PHY eval board II (top view without cover)

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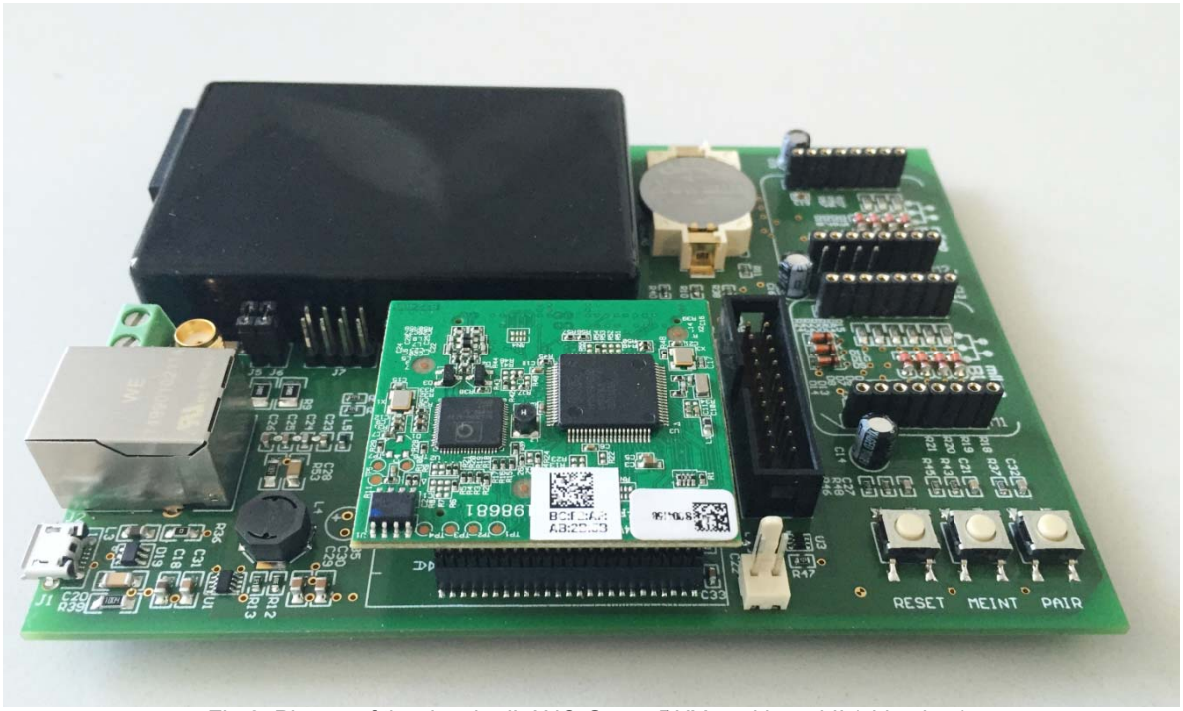

Fig 2: Picture of the devolo dLAN® Green PHY eval board II (side view)

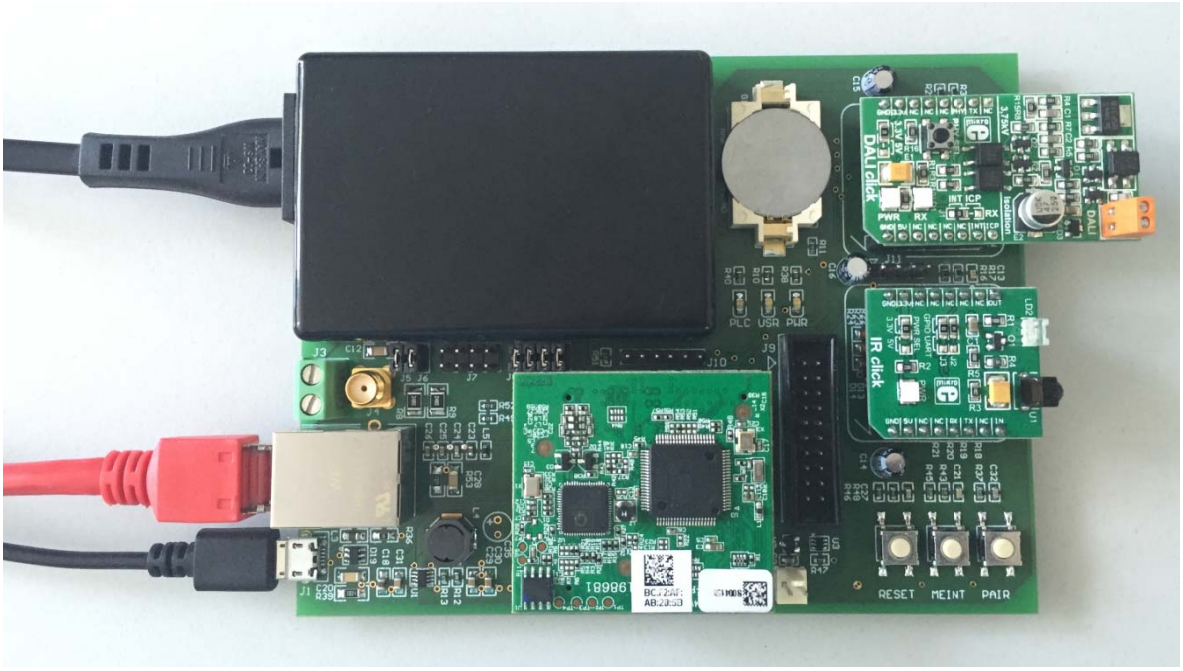

Fig 3: Picture of the devolo dLAN® Green PHY eval board II (with modules and connected)

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dLAN® Green PHY eval board II

1 Introduction

This data sheet gives you a short introduction in the major and most significant functions of this Evaluation Board. In this note acronyms are used for the whole Green PHY group like dLAN® Green PHY Module (GPM) and for dLAN® Green PHY eval board II (GPE).

The LPC1758 is running FreeRTOS and supports only PLC <-> Ethernet bridging at time of delivery. Advise: For firmware update of the LPC1758, one of the following interfaces should be made accessible:

- ➔ JTAG (see LPC17xx user manual)
- ➔ UART0 (see LPC17xx user manual)
- ➔ Ethernet (see dLAN@ Green PHY SDK manual)

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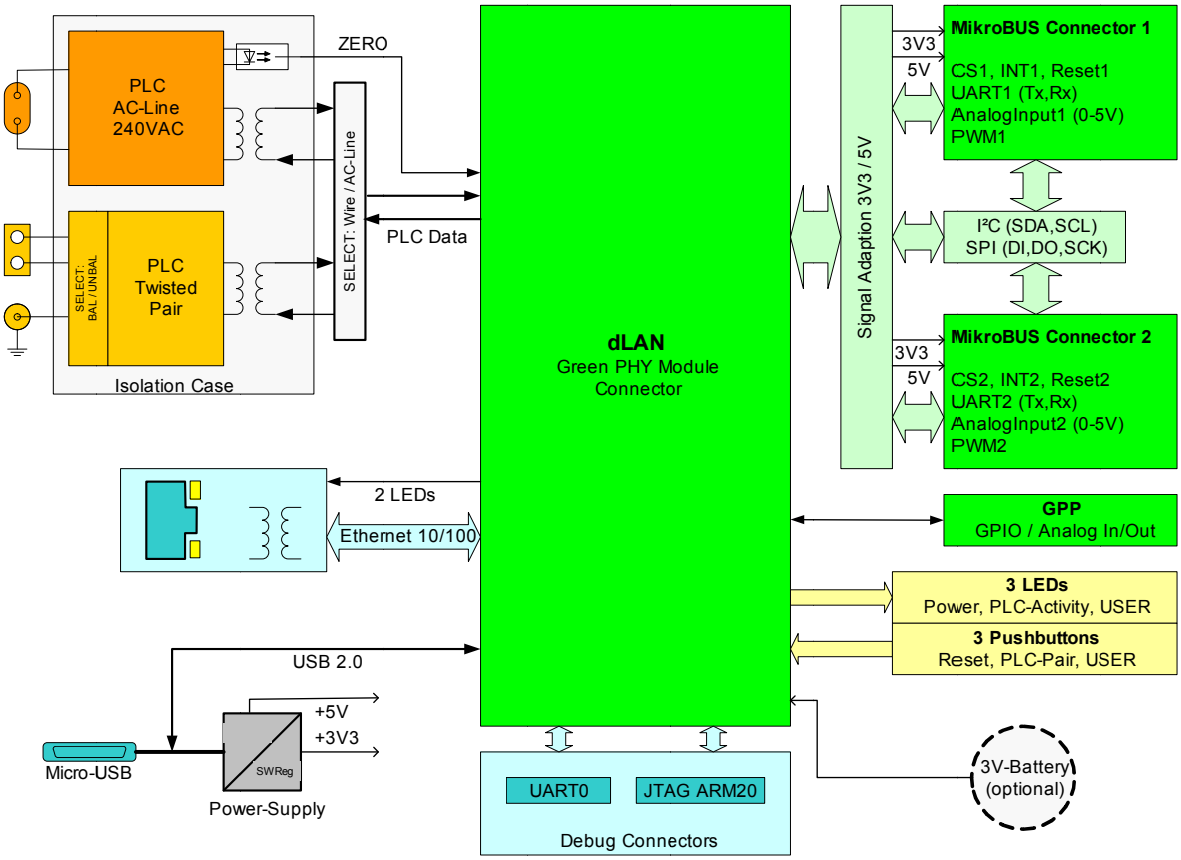

Fig 4: Block Diagram of the devolo dLAN® Green PHY eval board II

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2 Functionality of dLAN® Green PHY eval board II

This GPEB offers several interfaces connected to the pins of the GPM.

2.1 Power Connector (Micro-USB) – J1

Power Supply for the EVAL Board is provided by this Connector. Additional USB 2.0 Pins are connected to GPM's USB port and can be used if supported by special Software.

2.2 Fast Ethernet Connector (RJ45) – J2

Fast Ethernet RJ45 connector with integrated magnetics.

2.3 PLC Interfaces – AC, J3, J4

Power Line Communication interfaces are provided for AC-Line or for twisted pair lines.
AC-Line or twisted pair is selected alternatively by a jumper area (J8/J7). When twisted pair inputs are selected, you can choose between Screw-Terminal (J3) or a SMA Coaxial-Connector (J4).
AC-PLC-Circuits are protected by an isolation case.

2.4 UART0- Connector (1x6 Header) – J10

This connector can be used for Command-Line-Interface or just to get debug messages.
Programming the internal flash of the LPC1758 processor on the GPM (ISP-in circuit programming) is possible with special utilities. Pinout fits to standard FTDI USB-cable (3.3V-type).

2.5 JTAG Connector (2x10 Header) – J9

LPC1758 JTAG Interface with standard ARM20 pinout.

2.6 Pushbuttons – MRES, MINT, PAIR

Pushbutton PAIR is connected to GPIO3 of the QCA7000.
Default mode: initiate pairing mechanism.
MRES (manually Reset) initiates Hardware Reset circuitry,
MINT (manually Interrupt) is free for user demands.

2.7 LEDs – PWR, USR, PLC

PWR-LED (green) is connected to output of 3V3 switching regulator.
PLC-LED (green) reserved for signaling Power Line Communication activities.
USR-LED (yellow) is connected to an LPC port and free for user demands.

2.8 MikroBUS slots (2x8 Header) – M1, M2

Dual mikroBUS slots provide several communication lines and ports like TX, RX, SPI and TWI (I²C)
Many ready designed IO-modules using mikroBUS-layout are available from Mikroelektronika (www.mikroe.com/click) and other partners.

2.9 Two Wire Interface / I²C (1x4 Header) – J11

Separate connector with access to 3V3 power supply and I²C Interface lines.

2.10 GPP Digital/Analog (1x3 Header) – J12

General Purpose Port: GPIO, A/D and D/A, access to LPC1758 Port0[26].

2.11 Backup-battery 3V (optional) – G1

Optional VBAT supply for LPC1758's internal standby circuits and RTC.

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3 dLAN® Green PHY eval board II Pinout

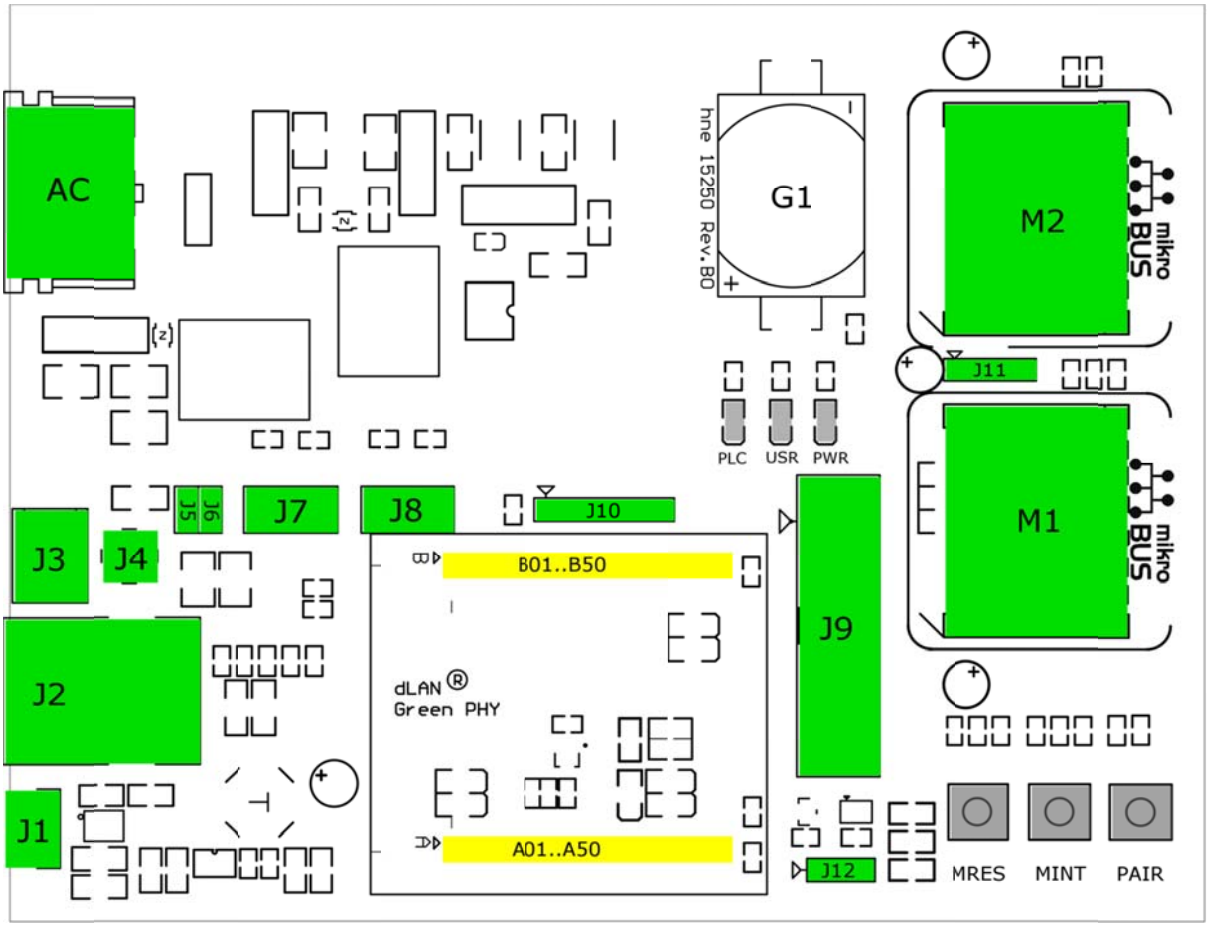

Fig 5: Top Assembly connectors marked

3.1 J1 – Pin Names USB (Micro-USB)

Pin No.	Pin Name	Type		USB Function
1	VUSB	P		**VCC:** +5V, 1A max
2	D-	I/O		**USB D-** connected to LPC1758 DM
3	D+	I/O		**USB D+** connected to LPC1758 DP
4	A/B	NC		**Not Connected**
5	GND	P		**Ground:** 0 V reference
S	Shield	S		**Shield:** connected to GND with 1nF//1M

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3.2 J2 – Pin Names Ethernet 10/100 (RJ-45)

Pin No.	Pin Name	Type	Ethernet Function
1	TX+	I/O	**TX+**
2	TX-	I/O	**TX-**
3	RX+	I/O	**RX+**
4		I/O	BIAS TX
5		I/O	
6	RX-	I/O	**RX-**
7		I/O	BIAS RX
8		I/O	
S	Shield	S	**Shield:** connected to GND with 1nF//1M

3.3 J3 – Pin Names PLC Twisted Pair (2Screw Terminal)

Pin No.	Pin Name	Type	PLC Function	Jumpers J7.1-J7.4 closed **Jumpers J8.1-J8.4 open !**
1	PLC+	I/O	**PLC+** Impedance 100Ω	J6 open
2	PLC-	I/O	**PLC-** balanced	J5 open

3.4 J4 – Pin Names PLC Coax (SMA female)

Pin No.	Pin Name	Type	PLC Function	Jumpers J7.1-J7.4 closed **Jumpers J8.1-J8.4 open !**
1	PLC+	I/O	**PLC+** Impedance 50Ω	J6 closed
2	PLC-	I/O	**PLC-** 1nF to GND	J5 closed

3.5 AC – Pin Names PLC AC-Line (C8P Connector)

Pin No.	Pin Name	Type	PLC Function	Jumpers J8.1-J8.4 closed **Jumpers J7.1-J7.4 open !**
1	AC	I/O	**240 VAC**	
2	AC	I/O	**240 VAC** this line is fused with 2A	

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3.6 J9 – Pin Names LPC1758 JTAG Connector (ARM20)

Pin No.	Pin Name	Type	JTAG Function	
1	3V3	P	**+3.3 V** supply voltage	
2	3V3	P	**+3.3 V** supply voltage	
3	TRST_N	I	**TRST** — Test Reset# for JTAG interface	
4	GND	P	**Ground:** 0 V reference	
5	TDI	I	**TDI:** Test Data In for JTAG interface	
6	GND	P	**Ground:** 0 V reference	
7	TMS/SWDIO	I I/O	**TMS/** **SWDIO:**	Test Mode Select for JTAG interface Serial Wire Debug Data Input/Output
8	GND	P	**Ground:** 0 V reference	
9	TCK/SWDCLK	I I	**TCK/** **SWDCLK:**	Test Clock for JTAG interface Serial wire clock
10	GND	P	**Ground:** 0 V reference	
11	RTCK	O	**RTCK:** Return Test Clock for JTAG interface Not supported, connected to GND over 10 kΩ	
12	GND	P	**Ground:** 0 V reference	
13	TDO/SWO	O O	**TDO/** **SWO:**	Test Data Out for JTAG interface Serial Wire trace Output
14	GND	P	**Ground:** 0 V reference	
15	SRST_N	OD	**SRST:** System Reset#	
16	GND	P	**Ground:** 0 V reference	
17	NC	NC	**Not Connected**	
18	GND	P	**Ground:** 0 V reference	
19	NC	NC	**Not Connected**	
20	GND	P	**Ground:** 0 V reference	

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3.7 J10 – Pin Names UART0 Debug Terminal (Header 1x6)

Pin No.	Pin Name	Type	UART Function
1	GND	P	**Ground:** 0 V reference
2	CTS	O	**connected to RTS via R51**
3	3V3	P	**+3.3 V** supply voltage for FTDI Cable (3.3V Type)
4	TXD	I	**Connected to UART0 RXD**
5	RXD	O	**Connected to UART0 TXD**
6	RTS	I	**connected to CTS via R51**

3.8 J11 – Pin Names I²C (Header 1x4)

Pin No.	Pin Name	Type	I²C Function
1	GND	P	**Ground:** 0 V reference
2	3V3	P	**+3.3 V** supply voltage
3	SDA	I/O	**SDA:** I²C Data line
4	SCL	I/O	**SCL:** I²C Clock line

3.9 J12 – Pin Names GPP (Header 1x3)

Pin No.	Pin Name	Type	Port Function
1	GND	P	**Ground:** 0 V reference
2	GPP	I/O	**GPIO / Analog-In/Out:** connected to Port P0[26]
3	3V3	P	**+3.3 V** supply voltage

3.10 M1, M2 – Pin Names mikroBUS Slots (Connector 2x8)

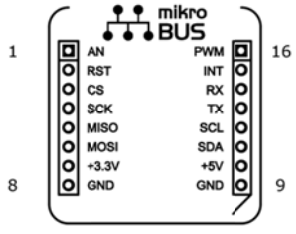

Fig 6: mikroBUS Port pin count

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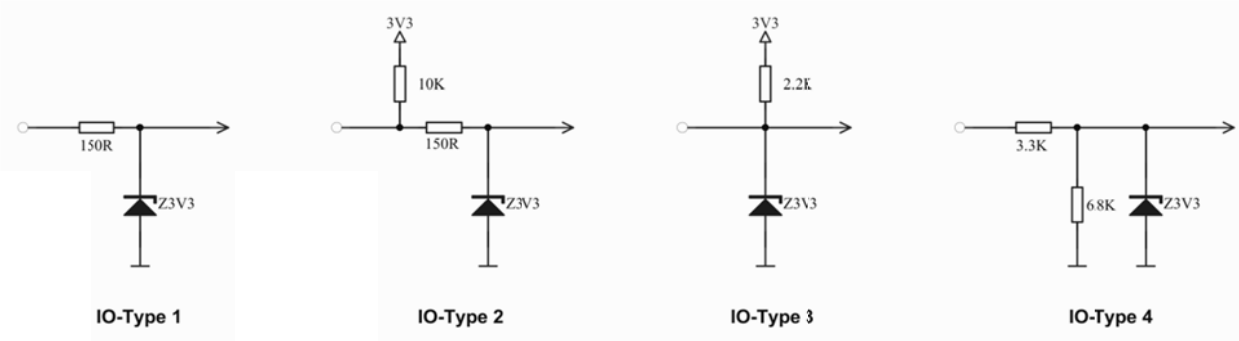

Fig 7.1 - 7.4: mikroBUS Port internal Connection Types

Pin No.	Pin Name	IO-Type	mikroBUS Function	Ports for M1	Ports for M2
1	AN	I-4	**Analog Port:** 0..5V	Port 1 [31]	Port 0 [25]
2	RST	O-2	**Reset# Pin**	Port 1 [26]	Port 1 [28]
3	CS	O-2	**SPI Chip Select#**	Port 2 [02]	Port 2 [07]
4	SCK	O-1	**SPI Clock Line**	Port 0 [07]	
5	MISO	I-1	**SPI Master Input**	Port 0 [08]	
6	MOSI	O-1	**SPI Master Output**	Port 0 [09]	
7	+3.3V	P	**+3.3 V** supply voltage		
8	GND	P	**Ground:** 0 V reference		
9	GND	P	**Ground:** 0 V reference		
10	+5V	P	**+5.0 V** supply voltage		
11	SDA	I/O-3	**I²C Data Line**	Port 0 [00]	
12	SCL	O-3	**I²C Clock Line**	Port 0 [01]	
13	TX	O-1	**UART Transmit**	Port 2 [00]	Port 0 [10]
14	RX	I-1	**UART Receive**	Port 2 [01]	Port 0 [11]
15	INT	I-1	**Interrupt# Input**	Port 2 [03]	Port 2 [06]
16	PWM	O-1	**PWM Output**	Port 2 [04]	Port 2 [05]

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3.11 dLAN® Green PHY Module – Row A Pin Names and Usage

Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
1	GND	P	**Ground:** 0 V reference	
2	VDD	P	**+3.3 V** supply voltage	
3	P0[11] / RXD2 / SCL2 / MAT3[1]	I/O I I/O O	**P0[11]** — General purpose digital input/output pin. **RXD2** — Receiver input for UART2. **SCL2** — I2C2 clock input/output **MAT3[1]** — Match output for Timer 3, channel 1.	M2: RX
4	P0[10] / TXD2 / SDA2 / MAT3[0]	I/O O I/O O	**P0[10]** — General purpose digital input/output pin. **TXD2** — Transmitter output for UART2. **SDA2** — I2C2 data input/output **MAT3[0]** — Match output for Timer 3, channel 0.	M2: TX
5	P2[2] / PWM1[3] / CTS1 / TRACEDATA[3]	I/O O I O	**P2[2]** — General purpose digital input/output pin. **PWM1[3]** — Pulse Width Modulator 1, channel 3. **CTS1** — Clear to Send input for UART1. **TRACEDATA[3]** — Trace data, bit 3.	M1: CS#
6	P2[7] / RD2 / RTS1	I/O I O	**P2[7]** — General purpose digital input/output pin. **RD2** — CAN2 receiver input. **RTS1** — Request to Send output for UART1.	M2: CS#
7	P2[4] / PWM1[5] / DSR1 / TRACEDATA[1]	I/O O I O	**P2[4]** — General purpose digital input/output pin. **PWM1[5]** — Pulse Width Modulator 1, channel 5. **DSR1** — Data Set Ready input for UART1. **TRACEDATA[1]** — Trace Data, bit 1.	M1: PWM
8	P2[5] / PWM1[6] / DTR1 / TRACEDATA[0]	I/O O O O	**P2[5]** — General purpose digital input/output pin. **PWM1[6]** — Pulse Width Modulator 1, channel 6. **DTR1** — Data Terminal Ready output for UART1. **TRACEDATA[0]** — Trace Data, bit 0.	M2: PWM
9	P2[3] / PWM1[4] / DCD1 / TRACEDATA[2]	I/O O I O	**P2[3]** — General purpose digital input/output pin. **PWM1[4]** — Pulse Width Modulator 1, channel 4. **DCD1** — Data Carrier Detect input for UART1. **TRACEDATA[2]** — Trace Data, bit 2.	M1: INT#
10	P2[6] / PCAP1[0] / RI1 / TRACECLK	I/O I I O	**P2[6]** — General purpose digital input/output pin. **PCAP1[0]** — Capture input for PWM1, channel 0. **RI1** — Ring Indicator input for UART1. **TRACECLK** — Trace Clock.	M2: INT#
11	P2[1] / PWM1[2] / RXD1	I/O O I	**P2[1]** — General purpose digital input/output pin. **PWM1[2]** — Pulse Width Modulator 1, channel 2. **RXD1** — Receiver input for UART1.	M1: RX
12	P2[0] / PWM1[1] / TXD1	I/O O O	**P2[0]** — General purpose digital input/output pin. **PWM1[1]** — Pulse Width Modulator 1, channel 1. **TXD1** — Transmitter output for UART1.	M1: TX
13	GND	P	**Ground:** 0 V reference	
14	VDD	P	**+3.3 V** supply voltage	
15	GND	P	**Ground:** 0 V reference	
16	P1[30] / VBUS / AD0[4]	I/O I I	**P1[30]** — General purpose digital input/output pin. **VBUS** — Monitors the presence of USB buspower Note: This signal must be HIGH for USB reset. **AD0[4]** — A/D converter 0, input 4.	USB: VBUS

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Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
17	P1[19] / MCOA0 / nUSB_PPWR / CAP1[1]	I/O O O I	**P1[19]** — General purpose digital input/output pin. **MCOA0** — Motor control PWM channel 0A. **nUSB_PPWR** — Port Power enable for USB port. **CAP1[1]** — Capture input for Timer 1, channel 1.	
18	P1[22] / MCOB0 / USB_PWRD / MAT1[0]	I/O O I O	**P1[22]** — General purpose digital input/output pin. **MCOB0** — Motor control PWM channel 0B. **USB_PWRD** — Power Status for USB port. **MAT1[0]** — Match output for Timer 1, channel 0.	
19	P2[9] / USB_CONN / RXD2	I/O O I	**P2[9]** — General purpose digital input/output pin. **USB_CONNECT** — Signal used to switch an external 1.5 k_ resistor under software control. Used with the SoftConnect USB feature. **RXD2** — Receiver input for UART2.	USB: MODE
20	P0[30] / USB_D−	I/O I/O	**P0[30]** — General purpose digital input/output pin. **USB_D−** — USB bidirectional D− line. A 33 Ohm resistor in series is integrated on Module.	USB: DN
21	P1[18] / USB_UP_LED / PWM1[1] / CAP1[0]	I/O O O I	**P1[18]** — General purpose digital input/output pin. **USB_UP_LED** — USB GoodLink LED indicator. **PWM1[1]** — Pulse Width Modulator 1, channel 1. **CAP1[0]** — Capture input for Timer 1, channel 0.	
22	P0[29] / USB_D+	I/O I/O	**P0[29]** — General purpose digital input/output pin. **USB_D+** — USB bidirectional D+ line. A 33 Ohm resistor in series is integrated on Module.	USB: DP
23	GND	P	**Ground:** 0 V reference	
24	VDD	P	**+3.3 V** supply voltage	
25	P1[25] / MCOA1 / MAT1[1]	I/O O O	**P1[25]** — General purpose digital input/output pin. **MCOA1** — Motor control PWM channel 1A. **MAT1[1]** — Match output for Timer 1, channel 1.	
26	RSVD		Reserved, do not connect.	
27	RSVD		Reserved, do not connect.	
28	RSVD		Reserved, do not connect.	
29	RSVD		Reserved, do not connect.	
30	RSVD		Reserved, do not connect.	
31	RSVD		Reserved, do not connect.	
32	RSVD		Reserved, do not connect.	
33	RSVD		Reserved, do not connect.	
34	RSVD		Reserved, do not connect.	
35	RSVD		Reserved, do not connect.	
36	RSVD		Reserved, do not connect.	
37	GND	P	**Ground:** 0 V reference	
38	VDD	P	**+3.3 V** supply voltage	
39	P0[26] / AD0[3] / AOUT / RXD3	I/O I O I	**P0[26]** — General purpose digital input/output pin. When configured as an ADC input or DAC output, the digital section of the pad is disabled. **AD0[3]** — A/D converter 0, input 3. **AOUT** — D/A converter output. **RXD3** — Receiver input for UART3.	GPP: General Purpose Port Digital / Analog (J12)

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Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
40	P1[31] / SCK1 / AD0[5]	I/O I/O I	**P1[31]** — General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **SCK1** — Serial Clock for SSP1. **AD0[5]** — A/D converter 0, input 5.	 M1: AN
42	P0[25] / AD0[2] / I2SRX_SDA / TXD3	I/O I I/O O	**P0[25]** — General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **AD0[2]** — A/D converter 0, input 2. **I2SRX_SDA** — Receive data. **TXD3** — Transmitter output for UART3.	 M2: AN
43	TDI	I	**TDI** — Test Data in for JTAG interface.	JTAG: TDI
44	VDD	P	**+3.3 V** supply voltage	
45	TMS / SWDIO	I I/O	**TMS** — Test Mode Select for JTAG interface. **SWDIO** — Serial wire debug data input/output.	JTAG: TMS
46	TDO / SWO	O O	**TDO** — Test Data out for JTAG interface. **SWO** — Serial wire trace output.	JTAG: TDO
47	TCK / SWDCLK	I I	**TCK** — Test Clock for JTAG interface. **SWDCLK** — Serial wire clock.	JTAG: TCK
48	nTRST	I	**nTRST** — Test Reset for JTAG interface.	JTAG: TRST#
49	GND	P	**Ground:** 0 V reference	
50	VDD	P	**+3.3 V** supply voltage	

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3.12 dLAN® Green PHY Module – Row B Pin Names and Usage

Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
1	GND	P	**Ground:** 0 V reference	
2	GND	P	**Ground:** 0 V reference	
3	G-PHY_ RXP	I	**RXP** — PLC Positive differential input.	PLC: RX+
4	G-PHY _TXP	O	**TXP** — PLC Positive differential output.	PLC: TX+
5	G-PHY _RXN	I	**RXN** — PLC Negative differential input.	PLC: RX-
6	G-PHY _TXN	O	**TXN** — PLC Negative differential output.	PLC: TX-
7	GND	P	**Ground:** 0 V reference	
8	GND	P	**Ground:** 0 V reference	
9	G-PHY_ZC_IN	I	**ZC_IN** — Zero Cross Input	PLC: Zero Crossing
10	RSVD		Reserved, do not connect.	
11	G-PHY _GPIO[0]	I/O	**GPIO 0** — Sets mode at power on, then becomes I/O.	PLC: Activity-LED#
12	G-PHY _GPIO[1]	I/O	**GPIO 1** — Sets mode at power on, then becomes I/O.	
13	G-PHY _GPIO[2]	I/O	**GPIO 2** — Sets mode at power on, then becomes I/O.	
14	G-PHY _GPIO[3]	I/O	**GPIO 3** — Sets mode at power on, then becomes I/O.	Button: PAIR
15	RSVD		Reserved, do not connect.	
16	RSVD		Reserved, do not connect.	
17	RSVD		Reserved, do not connect.	
18	RSVD		Reserved, do not connect.	
19	VDD	P	**+3.3 V** supply voltage	
20	RSVD		Reserved, do not connect.	
21	VDD	P	**+3.3 V** supply voltage	
22	GND	P	**Ground:** 0 V reference	
23	ETH_TXP	I/O	**TXP** – Ethernet Transmit Positive Channel	ETH: TDP
24	ETH_RXP	I/O	**RXP** – Ethernet Receive Positive Channel	ETH: RXP
25	ETH_TXN	I/O	**TXN** – Ethernet Transmit Negative Channel	ETH: TDN
26	ETH_RXN	I/O	**RXN** – Ethernet Receive Negative Channel	ETH: RXN
27	ETH_VDDCTX	O	**VDDCTX** – Ethernet XFMR CTX (Common Tap) Power supply.	ETH: CT Bias
28	ETH_VDDCTX	O	**VDDCTX** – Ethernet XFMR CTX (Common Tap) Power supply.	ETH: CT Bias
29	VDD	P	**+3.3 V** supply voltage	
30	GND	P	**Ground:** 0 V reference	
31	ETH_LED1	O	**LED1** – Sets mode at power on then becomes Ethernet Link/Activity LED indication (active High).	ETH: LED1
32	ETH_LED2	O	**LED2 –** Sets mode at power on then becomes Ethernet Link Speed LED indication (active Low). 100 = on, 10 = off.	ETH: LED2

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Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
33	P2[10] / nEINT0 / NMI	I/O I I	**P2[10]** — General purpose digital input/output pin. 5 V tolerant pad with 5ns glitch filter providing digital I/O functions with TTL levels and hysteresis. **Note:** A LOW on this pin while RESET is LOW forces the on-chip bootloader to take over control of the part after a reset and go into ISP mode. See LPC17xx user manual Section 32.1 for details. **nEINT0 —** External interrupt 0 input. **NMI —** Non-maskable interrupt input.	 Button: MINT
34	RSVD		Reserved, do not connect.	
35	P0[2] / TXD0 / AD0[7]	I/O O I	**P0[2] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **TXD0 —** Transmitter output for UART0. **AD0[7] —** A/D converter 0, input 7.	 UART0: TXD
36	P0[3] / RXD0 / AD0[6]	I/O I I	**P0[3] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **RXD0 —** Receiver input for UART0. **AD0[6] —** A/D converter 0, input 6.	 UART0: RXD
37	P0[8] / I2STX_WS / MISO1 / MAT2[2]	I/O I/O I/O O	**P0[8] —** General purpose digital input/output pin. **I2STX_WS —** Transmit Word Select. **MISO1 —** Master In Slave Out for SSP1. **MAT2[2] —** Match output for Timer 2, channel 2.	 SPI: MISO
38	P0[9] / I2STX_SDA / MOSI1 / MAT2[3]	I/O I/O I/O O	**P0[9] —** General purpose digital input/output pin. **I2STX_SDA —** Transmit data. **MOSI1 —** Master Out Slave In for SSP1. **MAT2[3] —** Match output for Timer 2, channel 3.	 SPI: MOSI
39	P0[6] / I2SRX_SDA / SSEL1 / MAT2[0]	I/O I/O I/O O	**P0[6] —** General purpose digital input/output pin. **I2SRX_SDA —** Receive data. **SSEL1 —** Slave Select for SSP1. **MAT2[0] —** Match output for Timer 2, channel 0.	 USR: User LED#
40	P0[7] / I2STX_CLK / SCK1 / MAT2[1]	I/O I/O I/O O	**P0[7] —** General purpose digital input/output pin. **I2STX_CLK —** Transmit Clock **SCK1 —** Serial Clock for SSP1. **MAT2[1] —** Match output for Timer 2, channel 1.	 SPI: SCK
41	P0[0] / RD1 / TXD3 / SDA1	I/O I O I/O	**P0[0] —** General purpose digital input/output pin. **RD1 —** CAN1 receiver input. **TXD3 —** Transmitter output for UART3. **SDA1 —** I2C1 data input/output see LPC17xx manual Section 19.1 for details.	 I2C: SDA
42	P0[1] / TD1 / RXD3 / SCL1	I/O O I I/O	**P0[1]** — General purpose digital input/output pin. **TD1** — CAN1 transmitter output. **RXD3** — Receiver input for UART3. **SCL1** — I2C1 clock input/output see LPC17xx manual Section 19.1 for details.	 I2C: SCL

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Pin No.	Pin Name	Type	Function on Module	Used on Eval as ...
43	V_{BAT}	P	**V_{BAT} —** RTC power supply If this pin is not powered, the RTC is still powered internally if VDD is present.	Connected to battery holder over 1KΩ
44	RSVD		Reserved, do not connect.	
45	P1[26] / MCOB1 / PWM1[6] / CAP0[0]	I/O O O I	**P1[26] —** General purpose digital input/output pin. **MCOB1 —** Motor control PWM channel 1B. **PWM1[6] —** Pulse Width Modulator 1, channel 6. **CAP0[0] —** Capture input for Timer 0, channel 0.	M1: RST#
46	P1[28] / MCOA2 / PCAP1[0] / MAT0[0]	I/O O I O	**P1[28] —** General purpose digital input/output pin. **MCOA2 —** Motor control PWM channel 2A **PCAP1[0] —** Capture input for PWM1, channel 0. **MAT0[0] —** Match output for Timer 0, channel 0.	M2: RST#
47	nRSTOUT	O	**nRSTOUT —** This is a 3.3 V pin. A LOW output on this pin indicates that the device is in the reset state, for any reason. This reflects the RESET input pin and all internal reset sources.	
48	nRESET	I	**nRESET —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.	Button: MRES
49	VDD	P	**+3.3 V** supply voltage	
50	GND	P	**Ground:** 0 V reference	

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dLAN® Green PHY eval board II

4 dLAN® Green PHY eval board II Specifications

- Board Dimensions with GPM, no mikroBUS modules: 130 mm x 100 mm x 22 mm

Symbol	Parameter	Min	Typ	Max
$T_{OPERATE}$	Operation Temperature	0°C		70°C
V_{SUPPLY}	Supply Voltage	4.75 V	5V	5.25 V
I_{SUPPLY}	Supply Current @5.1 V with GPM *[1]		0.32 A	0.52 A

The dLAN® Green PHY Module (GPM) is plugged into the Evaluation Board sockets **A** and **B**. For the dLAN® Green PHY Module specification, please see the dLAN® Green PHY Module data sheet.

*[1] If mikroBUS IO-Modules are plugged additionally into the Evaluation Board sockets **M1** and **M2**, their power consumption will increase the supply current. Please refer to the appropriate data sheets.

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dLAN® Green PHY eval board II

5 Revision History

Revision	Modifications
1.0	• Original Issue

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